

CmpSci 201

Homework 11

1. Given a 1 GHz processor ($1 * 10^{-9}$ sec/cycle), a main memory access time of 100ns (100 cycles), and one level of cache with 85% **hit rate** and an access time of 10ns, what is the average memory access time?
2. With the same configuration as above, what would the **miss rate** have to be in order for the average access time to be 15ns?
3. Given a 2-way set associative cache with 4K lines (2^{12} lines), if the cache has 8 words per line:
 - (a) How many bytes are there per line?
 - (b) How many bytes are there in the cache altogether?
 - (c) How many ways are there?
 - (d) How many sets are there in the cache altogether?
4. Assuming a completely empty fully associative cache and a 4 word line size (16 bytes per line), mark which of the following memory accesses (in the order given) will cause cache misses. Don't forget that the cache starts empty!

0x00000001
0x00000000
0xCAFEBA0
0x00000002
0xCAFEBAAF
0xCAFEBA03
0xCAFEBAAD

5. Given a direct mapped write-no allocate cache (where lines from memory are **NOT** brought in on a cache write miss), work through the following short ARM program, showing the state of cache and memory after execution.

```
MOV    R0, #4
MOV    R1, #7
LDR    R4, [R0]
LDR    R5, [R1]
ADD    R4, R4, R5
MOV    R1, #hC
LDR    R6, [R1]
STR    R4, [R0]
MOV    R1, #hF
STR    R6, [R1]
```

(diagram is on the next page)

