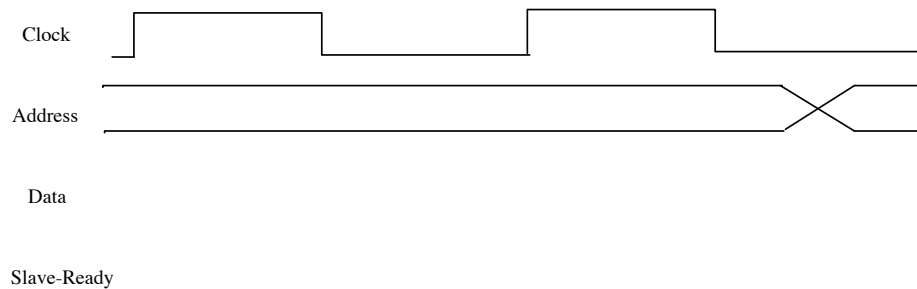


CmpSci 201

Homework 8

1. On a synchronous bus with support for multi-cycle data transfer, the master asserts the address and command lines and the slave transmits the data. Because the data may take multiple cycles to be sent, the slave asserts the slave-ready line when it starts the transmission and then de-asserts it when the transmission is over. Given the following timing diagram, assuming that the master has already sent address and command information, add timings for a slave device that starts transmitting in cycle 0 but doesn't finish until cycle 1 (but before address changes again).



2. Consider the following bus: a server has a central controller card, but devices are attached to this card with cables. Each device is equipped with pass-through circuitry and an additional connector, so to add another device to the bus you just plug it into the last device. This is called daisy-chaining and is used by SCSI (as well as other systems). Assuming that you have to support many devices (more than 8) and that these devices may be separated by many inches of cabling:
 - (a) Would you implement the bus as a synchronous or asynchronous bus? Why?

- (b) Would you use centralized or distributed arbitration? Why?

3. Given a memory with 8-bit words, and only 16 addressable words (4 address bits), trace out the basic memory organization for a 4x1 memory system (that is the row decoder takes 4 bits, and there is no column decoder). *Note: you do not have to trace out the individual boolean gates, just draw a trapezoid and label it a decoder*

4. Given a memory with 8-bit words, and only 16 addressable words (4 address bits), trace out the basic memory organization for a 2x2 memory system.

5. On a system with 32-bit addresses (like your home/dorm computer), if there is only 512 MB of memory, how many bits do you need to address any byte?
6. Assuming that the 512MB of RAM are all implemented in the same cell array:
- (a) If you split the necessary address bits in half (or as near as possible), how many bytes are stored in each line?
 - (b) If you split the necessary address bits in half (or as near as possible), how many lines would the cell array have?
 - (c) Sketch out a memory organization that splits the necessary address bits in half. *Note: I'm looking for a diagram like Figure 5.7 out of the book, you don't need to draw the individual cells*