



CSC 262: Homework 8
Due Dec. 9

1. Assume 32-bit addresses. On a system with 16K pages, how many bits are needed to store the page offset? How many bits are needed to store the page number?
2. Given 32-bit addresses and 16K pages. If you divide the page number bits evenly, how many bits are needed for each level with 2 level paging? 3 level paging?
3. Given 64 bit addresses and 8K pages, how many bits per level using 3-level paging?
4. Given 64 bit addresses, 8K pages, and three-level paging how large are each of the page tables (given 8 bytes per entry)?
5. The following questions ask you to perform simulations of page replacement policies. The simulation is of a process with access to only 3 pages of physical memory, however the process requires 6 pages. The address trace is as follows: 1, 2, 2, 3, 6, 5, 1, 4, 3, 2, 5, 3. Write the virtual page number inside the box corresponding to the physical page. Denote a page fault by circling the replaced page.

A) What would the trace be for OPT?

time 

B) What would the trace be for FIFO?

time 

C) For LRU?

time 