CMPSCI 201 – Spring 2004 Review and Study Guide for Midterm #1 Professor William T. Verts

Machine Models	Program Creation
One Address (e.g., 6502)	Editing Text
Two Address (e.g., 8088)	Assembling
Three Address (e.g., ARM)	Linking
RISC vs. CISC	Running (in Emulator)
Little-Endian vs. Big-Endian	
Register-Memory operations	Subroutine Issues
Register-Register operations	Return Address Management
Fetch-Execute Cycle	Register Transparency
Program Counter	Passing Parameters
RAM Memory Layout, Addressing	Through Registers
Subroutine Return Address Styles	Through Memory
First Word of Subroutine	
Pushed on Stack	ARM Registers
Stored in Register	16 Integer: R0-R15 (including LR, PC,)
	8 Floating: F0-F7
Numeric Formats & Conversions	CPSR (NZVC flags)
Conversions: decimal – hex – binary	
Naturals (unsigned integers)	Storage Allocation
Integers (signed)	DCD (word)
Fixed Point	DCFS (single, float)
Floating Point	DCFD (double, float)
Single Precision	
Double Precision	Instruction Formats
Extended Precision	Op Codes
	Conditional Execution
Binary Arithmetic	Setting Status Flags
Addition	Integer Constants (value plus right-rotate)
Subtraction	Registers with Shift/Rotate
Shifting Bits	
Logical Shift	Memory Instructions
Arithmetic Shift	LDR / STR
Rotating Bits	LDFS / STFS
Negating (2's complement)	LDFD / STFD
Masking (AND, OR, EOR)	
Generation and Use of Carry	Integer Arithmetic and Test Instructions
Detection of Zero	MOV / MVN
Detection of Negative	ADD / ADC / SUB / SBC / RSB / RSC
Detection of Overflow	AND / ORR / EOR / BIC
	CMP / CMN / TST / TEQ
Storage Sizes	MUL / UMULL
Byte	
Word	Floating Point Instructions
Floating Single	ADF / SBF / MUF / DVF / RSF / RDF
Floating Double	ABS / POW / RPW / SQT
	CMF / FLT / FIX
Language Structures	Constants $0.0 - 5.0$, 10.0 , 0.5
While loops	
Repeat loops	Branches and Conditions
If-Then	B / BHI / BLS
If-Then-Else	BEQ / BNE / BMI / BPL
	BCC / BCS / BVC / BVS
	DCT / DCE / DLT / DLE

 $BGT \, / \, BGE \, / \, BLT \, / \, BLE$